

AQA Computer Science A-Level
4.6.4 Logic gates
Concise Notes



Specification:

4.6.4.1 Logic gates:

Construct truth tables for the following logic gates:

- NOT
- AND
- OR
- XOR
- NAND
- NOR

Be familiar with drawing and interpreting logic gate circuit diagrams involving one or more of the above gates.

Complete a truth table for a given logic gate circuit.

Write a Boolean expression for a given logic gate circuit.

Draw an equivalent logic gate circuit for a given Boolean expression.

Recognise and trace the logic of the circuits of a half-adder and a full-adder.

Construct the circuit for a half-adder.

Be familiar with the use of the edge-triggered D-type flip-flop as a memory unit.

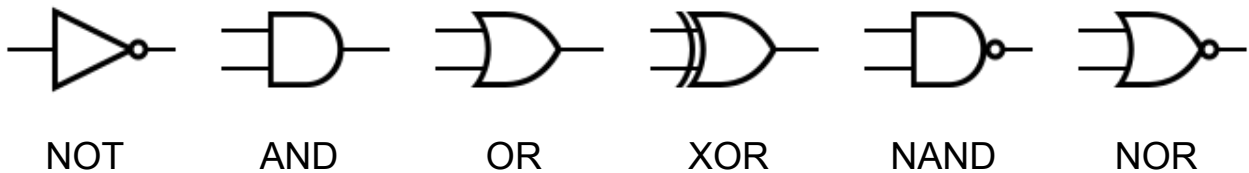


Logic Gates

- Billions of them make up **processors**
- Apply **logical operations** to one or more **Boolean inputs**
- Produce a **single output**
- Can be **combined** to form **logic circuits**

Logic Gate Symbols

- Logic gate symbols are **internationally recognised**
- **Inputs** are on the **left**
- **Outputs** are on the **right**



Truth Tables

- Show **every possible combination** of inputs and the **corresponding output**
- Inputs are **labelled alphabetically** starting with A
- The output is usually labelled **Q**

NOT

- **One input** and **one output**
- The output is always **the opposite** of the input

A	Q
0	1
1	0

$$Q = \bar{A}$$



AND

- Has **two inputs**
- Outputs the **product** of the two inputs
- Only outputs TRUE when **both inputs** are TRUE

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

$$Q = A \times B$$

OR

- Has **two inputs**
- Outputs the **sum** of its inputs
- Only outputs FALSE when **both inputs** are FALSE

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

$$Q = A + B$$



XOR

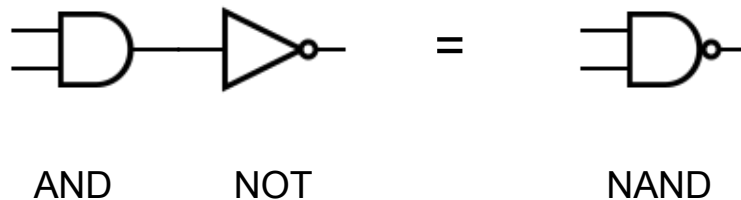
- Short for **exclusively or**
- Outputs TRUE when **strictly one** input is TRUE
- Has the symbol \oplus

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

$$Q = A \oplus B$$

NAND

- Short for **NOT AND**
- A **combination of two gates**: NOT and AND
- The same as AND, but with **reversed** output



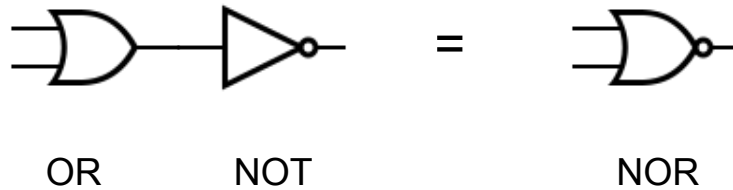
A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

$$Q = \overline{A \times B}$$



NOR

- Short for **NOT OR**
- A **combination** of NOT and OR
- The same as OR, just with the output **reversed**



A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

$$Q = \overline{A + B}$$

Combining Logic Gates

- Logic gates can be **combined** to form **more complex** circuits
- In order to create a truth table for a logic circuit:
 1. Fill in a table with **all the possible permutations of inputs**
 2. **Add columns** for each of the **elements** that make up the **final output** until you have made a column for the final output
 3. **Remove columns** used for working
 4. **Rename** the final column **Q**

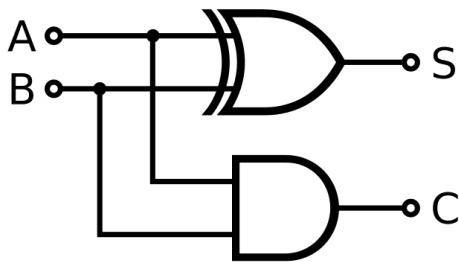


Adders

- A **logic circuit** that can be used to **add Boolean values**
- **Two types:**
 1. Half adders
 2. Full adders

Half adders

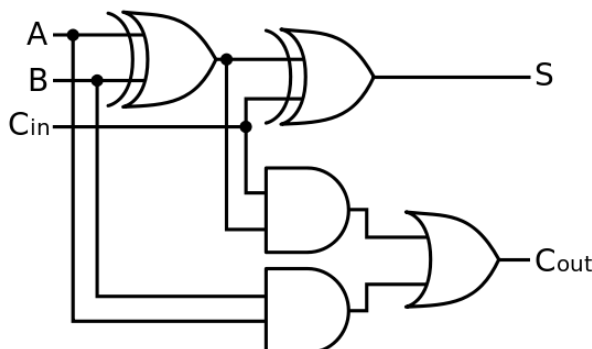
- **Two inputs**, **two outputs** and **two logic gates**
- Used to **add two Boolean values**
- Inputs labelled **A** and **B**
- Outputs labelled **S** and **C**
- **S** and **C** are short for **sum** and **carry**



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full adders

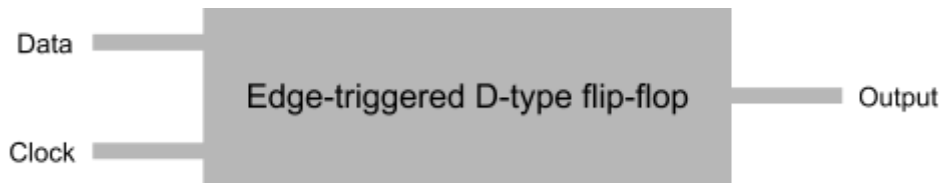
- **Three inputs** labelled **A**, **B** and **C_{in}** for **carry in**
- **Two outputs** labelled **S** for **sum** and **C_{out}** for **carry out**
- Can input two Boolean values **and a carry bit**
- **Carry bit taken** from a previous, **less significant** operation



A	B	C _{in}	S	C _{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Edge-triggered D-type flip-flop



- Can be used as a [memory unit](#)
- Stores the value of a [single bit](#)
- [Two inputs](#), one for [data](#) and another for a [clock signal](#)
- The clock signal:
 - [Is generated by the computer](#)
 - [Alternates](#) between 0 and 1
 - Alternates at a set [frequency](#)
 - Can be used to [synchronise](#) numerous flip-flops when they form part of a [larger system](#)
- [One output](#), which holds the [value of the stored bit](#)
- The value of the stored bit is [set](#) with each [change](#) of the clock signal

